REMARKS

Claims 1-36 were examined in the outstanding final office action mailed on 06/15/2005 (hereafter "Outstanding Office Action"). Claims 1-4, 9-13, 18-28 and 33-36 were rejected under 35 U.S.C. 103 (a) as being unpatentable over United States Patent Application 6,424,629 naming as inventor Rubino et al (hereafter "Rubino"), and claims 5-8, 14-17, and 29-32 were indicated to be allowable if rewritten in independent format. Applicants thank the Examiner again for indication of the allowable subject matter.

However, Applicants respectfully traverse the rejection with respect to the rejected claims 1-4, 9-13, 18-28 and 33-36.

It is applicants position that the Examiner is using impermissible hindsight in arguing that Rubino renders the rejected claims obvious under 35 U.S.C. § 103.

For example, independent claim 1 recites in relevant parts that:

> receiving in said first end system a plurality of loopback command packets from said another end system on said bi-directional virtual circuit;
> ***sending from said first end system a plurality of loopback response*** packets to said another end system, wherein said another end system determines that said bi-directional virtual circuit is operational based on the reception of said plurality of said response packets; and
> concluding ***in said first end system*** that said bi-directional virtual circuit is operational according to the determination of said another end system.
> (Original Claim 1, ***Emphasis Added***)

Thus, a first end system ("End System A") in accordance with claim 1 sends loopback response packets to another end system ("End System B"). End System B determines the operational status of the bidirectional virtual circuit and End System A then concludes that the bi-directional virtual circuit is operational according to the determination of End System B.

Turning to Rubino, as also seems to be appreciated by the Examiner, it is first noted that Rubino discloses (using the terminlogy of End Systems A and B) that End System A sends loopback response packets and that End System B determines the operational status of a virtual circuit (the bidirectional virtual circuit). End System B updates the routing information in another

layer (e.g., network layer) and "the routing information" (see below paragraphs) is propagated to End System A.

Contrary to the assertion in the Outstanding Office Action, there is no disclosure or suggestion in Rubino to conclude in End System A that the bi-directional virtual circuit is operational based on the routing information (or other layer information) received from End System A. The Examiner is simply impermissibly basing the conclusion of obviousness with the benefit of the disclosure of the subject patent application.

In support of the above assertion, Applicants note:

(1) the art of record does not establish that content of the "routing information" sent to End System A of Rubino at least facilitates a conclusion that the bidirectional virtual circuit is operational; and

(2) even if the routing information facilitates such a conclusion, there is simply no disclosure or suggestion in the art of record to make the claimed conclusion in End System A.

With respect to (1) above, Rubino discloses in relevant parts:

> Upon detecting the failure of the logical connection, the ATM Layer Logic 1008 sends a signal to the Network Layer Logic 1006 over the interface 1018 indicating that the logical connection failed. This prompts the Network Layer Logic 1006 to ***delete the logical connection from the routing table 1012 over the interface 1020, which in turn prompts the Routing Protocol Logic 1004 to select an alternate logical connection, update the routing table 1012 to re-route information to the alternate logical connection, and advertise the updated routing information to the other ATM routers***.

(Col. 9 line 60 - Col 10 line 3 of Rubino, ***Emphasis Added***)

Rubino appears to be silent as to the content of the "routing information" sent to other ATM routers. For example, the routing information is not expressly described as including information on the status of the failed logical connection (or alternative information that would facilitate the claimed conclusion).

Without sufficient information in the routing information, it appears that End System A ("other ATM routers") of Rubino will not be able to make the claimed

conclusion on the operational status of the bidirectional virtual circuit. The art of record does not appear to provide sufficient basis which facilitates the claimed conclusion to be made.

The burden of coming forward with clear evidence and logical reasoning rests with the Patent Office, and the burden is not met.

With respect to (2) above, it is noted that the description (including Figures 10A - 10C, relied upon by Examiner in lines 10-17 Page 11 of the Outstanding Office Action) of Rubino relates substantially to End System B (and not to End System A, where the claimed conclusion is made according to claim 1), and sufficient disclosure/suggestion appears to lack in Rubino with respect to making the claimed conclusion in End System A.

The Examiner is respectfully requested to point to the specific disclosure (i.e., sufficient processing) in Rubino (or other art of record) which discloses or suggests that the routing information is (can be) used in making the claimed conclusion (e.g., regarding the PVCs of Rubino).

From the above, it is respectfully asserted that it would not be obvious to modify the embodiments of Rubino to provide the claimed features of claim 1. Accordingly, previously presented claim 1 is patentable over the art of record.

Applicants now traverse the rejection with respect to previously presented claim 2. With respect to claim 2, it was stated in the Outstanding Office Action that:

> However, Rubino et al disclose that an ATM router 102 repeatedly ***receives AIS signals at a frequency of one-second intervals while a PVC failure persists***. The ATM router 102 determines that the PVC is operational once it stops receiving AIS signals for a predetermined time, preferably three seconds. Refer to Column 6, lines 37-57. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include examining a receive frequency at

> which said plurality of loopback command packets are received and determining that said bi-directional virtual circuit is operational if said receive frequency does not change substantially, the motivation being so that an end router will be able to determine when a failure occurs and when the failure is restored based on the rate of the loopback signals.
> (Page 3 line 16 to page 4 line 3 of Rubino, ***Emphasis Added***)

Thus, the Examiner appears to rely on AIS signals of Rubino in rejecting claim 2. With respect to claim AIS signals it was noted in Rubino that:

> Alarm surveillance is a mechanism by which the ATM router is explicitly notified when a PVC failure occurs. With reference to FIG. 3, the ATM switch 106 monitors the status of the PVC 110. ***When the ATM switch 106 detects the PVC failure 112, the ATM switch 106 transmits an Alarm Indication Signal (AIS) 114 to the local ATM router 102***. Upon receiving the AIS 114, the local ATM router 102 may, but is not required to, transmit a Far End Receive Failure (FERF) signal 115 (also referred to as a "Remote Defect Indication" signal). The purpose of the FERF signal 115 is to notify any intermediate nodes between the local ATM router 102 and the ATM switch 106 (not shown in the figure) that the PVC 110 has failed.
> (Col 5 lines 53-65 of Rubino, ***Emphasis Added***)

From the above, it is noted that the AIS signals of Rubino are generated by an intermediate ATM switch, and not by end systems between which the PVC (bidirectional virtual circuit) is provisioned. In addition, the AIS signals are generated only upon PVC failure.

In sharp contrast, the claimed loopback packets are between the two end systems between which the bidirectional virtual circuit is provisioned (as can be seen from claim 1). In addition, end system B determines that the virtual circuit is operational based on the reception of loopback response packets as recited in claim 1.

Due to the use of the loopback packets between the two end systems (and covering the entire path of the virtual circuit), the status of the bidirectional virtual circuit can be detected more reliably.

Accordingly, claim 2 is also independently allowable over the art of record. Claims 10, 11, 21, 22, 25, 26 are also independently allowable over the art of record for reasons similar to those noted above. The dependent claims are allowable at least as depending from corresponding base claim(s).

Thus, all the claims presented for consideration are believed to be in condition for allowance. The Examiner is invited to telephone the undersigned representative if it is believed that an interview might be useful for any reason.

Respectfully submitted,

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